Remarks

Upon entry of the present Reply, claims 1-24 are pending in the present application. New claims 23 and 24 are added herein. Support for new claim 23 may be found, for example, at p. 17, lines 4-7 and in Fig. 5. Support for new claim 24 may be found, for example, at p. 17, line 33 to p. 18, line 5. Thus the new claims are fully supported in the application as originally filed and contain no new matter.

Rejections of Claims over Tamm et al. in view of Tsushima And Tertiary References.

All of the pending claims stand rejected as obvious over Tamm et al., US 5666722 in view of Tsushima, US 2004/0086806, and Chang et al., US 5774340 or McCormack et al., US 2002/0175402, and in one case (claim 16) further in view of Konrad et al., US 2002/0129972, and in one case (claim 17), further in view of Yokogawa, US 6740416. Applicant respectfully traverses these rejections of the claims, and requests reconsideration and withdrawal of said rejections, for at least the following reasons.

Applicants respectfully submit that the references fail to disclose or suggest all of the features of claim 1 of the present application. Accordingly, there is no basis for a *prima facie* case of obviousness, and the rejections of Applicants' claims should be withdrawn.

According to the Office action, Tamm discloses all steps of the method set out in claim 1 including providing a printed circuit board, but admits the exceptions that Tamm does not disclose:

(a) providing a printed circuit board having circuit traces on at least one side thereof,

(b) the trenches not extending completely through the dielectric layer and

(c) depositing a primer layer into the produced trenches and vias only;

(d) the vias extending through the dielectric layer to the circuit traces.

The Office action contends that Tsushima discloses the limitation (b) above, *i.e.*, that the trenches do not extend completely through the dielectric, and the limitation (c), *i.e.*, that a primer layer is deposited into the produced trenches. The

Office action concludes that it would have been obvious to one of ordinary skill to utilize in Tamm the trenches not extending completely through the dielectric layer and depositing a primer layer into the produced trenches and vias only.

The Office action further contends that Chang et al. discloses the limitation (a) above, *i.e.*, the step of providing a printed circuit board having circuit traces on at least one side thereof, and the limitation (d), *i.e.*, that the vias extend through the dielectric layer to the circuit traces.

Alternatively, the Office action contends that McCormack et al. discloses the limitation (a) above, *i.e.*, the step of providing a printed circuit board having circuit traces on at least one side thereof, and the limitation (d), *i.e.*, that the vias extend through the dielectric layer to the circuit traces.

As to Chang et al. and McCormack et al. above, the Examiner concludes that it would have been obvious to one of ordinary skill to utilize in Tamm a printed circuit board having circuit traces on at least one side thereof and the vias extending through the dielectric layer to the circuit traces.

However, Applicants respectfully submit that the foregoing statements of the Examiner regarding claim 1 contain substantial errors regarding the teachings of the cited references:

- Tamm does not disclose a printed circuit board and coating the circuit board on the at least one side thereof with a dielectric:

To the contrary of the Office action contention, Tamm's substrate is a dielectric insulating dielectric foil 20 (col. 4, lines 62-63), whereas a printed circuit board is a structure which comprises, in addition to dielectric layers, circuit traces which serve to connect any electronic components mounted thereon with each other:

> *"A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, tracks or traces etched from copper sheets laminated onto a non-conductive substrate. It is also referred to as printed wiring board (PWB) or etched wiring board."* (Wikipedia: "printed circuit board")

As Tamm's substrate does not have any conductive pathway, tracks or traces

which could electrically connect electronic components, it is not a printed circuit board.

- Tsushima does not disclose producing traces by using laser ablation:

To the contrary of the Office action contention, Tsushima teaches using a photosensitive layer 2 which is subjected to a radiation so that an exposed portion is formed. Thereafter the exposed portions are exposed to an aqueous alkaline solution or the like to dissolve away the exposed portion and to form a channel portion ([0027], [0029]). Contrary to this, laser ablation refers to direct removal of material by the action of a laser without mediation of a chemical agent which would be responsible for removing the material:

> *Laser ablation is the process of removing material from a solid (or occasionally liquid) surface by irradiating it with a laser beam. At low laser flux, the material is heated by the absorbed laser energy and evaporates or sublimates. At high laser flux, the material is typically converted to a plasma. Usually, laser ablation refers to removing material with a pulsed laser, but it is possible to ablate material with a continuous wave laser beam if the laser intensity is high enough."* (Wikipedia: "laser ablation")

Accordingly, Tamm does not teach the general structure of the high density circuit carrier as a substrate to which the dielectric with trenches and vias is coated as set out in claim 1 of the present application because Tamm's circuit board does not have in the interior thereof a structure having circuit traces but is simply a dielectric layer. Therefore, Tamm's final product is a circuit board having on each of both sides circuit traces and, in addition, vias connecting the circuit traces on the different sides, whereas the product obtained with the method of the present invention is a circuit carrier which has in the interior a structure which comprises circuit traces and itself already forms an interconnection board and, in addition, which has on at least one of the outer sides further circuit traces.

The reason to form the construction of the present invention is very important:

A conventional printed circuit board may be used as the primary board to thereafter produce thereon very fine circuitry. This procedure is very advantageous

because almost all circuitry may be included into the conventional printed circuit board which may be manufactured at low cost because the conventional techniques to manufacture such boards are well-established and will be produced at a very high yield. The additional electrical connection layers to be produced on the outer sides of this conventional board are made to match high-density electronic components like semiconductor chips in flip-chip assembly which require small-pitch circuitry to be electrically connected to the board. Conventional circuit boards are not suitable to provide electrical connection to such small-pitch electronic components, but circuitry formed with laser ablated trenches and vias is suitable. By separating the two manufacturing sequences – manufacturing the conventional board in a first sequence and manufacturing the outer electrical connection layer in a second sequence on the conventional board – offers the advantages of parallel manufacture, *i.e.*, if the conventional board is scrap, not the whole circuit carrier will be scrap, and of cost-effective manufacture because most of the interconnection will be incorporated into the conventional board and can therefore be manufactured at low cost, whereas only those portions of the circuit carrier which require fine-pitch circuitry are manufactured with the sequence of method steps (b) through (f) as set out in claim 1. For a more detailed discussion of the advantages, Applicants respectfully refer the Examiner to page 10, line 18 through page 12, line 2 and page 13, lines 11-26 of the present specification. The important advantages of the presently claimed invention are clearly disclosed and related to the steps of the claimed method.

Applicants respectfully disagree and submit there is no substantial evidence to support the conclusion in the Office action that it would have been obvious to one of ordinary skill to utilize in Tamm the trenches not extending completely through the dielectric layer as in Tsushima if in method step (a) of the invention a printed circuit board having circuit traces on at least one side thereof is used as in Chang et al. or in McCormack et al.

The reason, according to the present invention, that the trenches are designed not to extend completely through the dielectric layer which is provided over the circuit traces of the circuit board (method step (b) in the method claim 1) is that the conductor lines formed in the trenches are not to connect to the circuit traces

underneath these conductor lines in order to prevent an electrical short.

The reason Tsushima designs his channel portions 2b to not connect to the substrate 1 is due to the fact that Tsushima wants to change the nature of the material at the bottom of these channel portions 2b such that palladium nuclei are formed there so that, once the palladium nuclei are formed, metal may be deposited by electroless deposition in the channel portion 2b:

Tsushima states in paragraphs [0030] and [0031] that a mask 3 is positioned such that its open pattern is brought into register with the channel portion 2b of the photosensitive layer 2 and that, by this arrangement, an inside of the channel portion 2b can be exposed to an ultraviolet radiation 4 so that an exposed portion 2c can be formed in the channel portion 2b of the photosensitive layer 2, as shown in Fig. 2 (e), and that further a palladium salt containing liquid is brought into contact with the exposed portion 2c to thereby form palladium nuclei in this exposed portion 2c by chemical reduction.

It is to be kept in mind in this respect that Tsushima teaches forming a metal pattern on a substrate ([0010]), which implies that this substrate is a dielectric because otherwise the metal pattern could not be used as an electrical connecting structure in a circuit board ([0009]). In the figures this substrate is referenced with numeral 1 ([0026]). There is no need in Tsushima hence that the channel portion 2b with exposed portion 2c be spaced apart from this substrate which would otherwise be necessary if the substrate would have exposed circuit traces or would be a metal plate or the like in order to prevent any electrical short.

Accordingly, Tsushima's process is completely different from the present invention where a printed circuit board is used as a substrate which of course has circuit traces on at least one surface thereof and which is coated on the at least one side thereof with a dielectric over the circuit traces. In this case, the conductor lines formed in the trenches must be spaced apart from the circuit traces in order to prevent an electrical short between the conductor lines in the trenches and the circuit traces.

Using the technique taught by Tsushima is not suited to be used with a printed circuit board as a substrate which has circuit traces provided on at least one surface thereof, as in Chang et al. or in McCormack et al. This is because the

exposed portion 2b which has been contacted with the palladium salt containing solution and which therefore contains palladium nuclei therein will evidently create an electrical short between the metal film 5 formed in the channel portion 2b (Fig. 2 (g)) and the circuit traces of a printed circuit board used instead of the substrate 1 via the palladium nuclei contained in the exposed portion 2c.

For this reason, those skilled in the art would not have contemplated combining Tamm with Tsushima and with Chang et al. or with McCormack et al.

Claim 12: Tsushima Does Not Disclose or Suggest Sputtering

Regarding claim 12, the Office action once again incorrectly contends that Tsushima discloses a sputtering method. This is wrong, clearly erroneous and not only without support of substantial evidence, but in fact contrary to the teachings of Tsushima. The word "sputtering" does not appear in Tsushima. No process step that could possibly be construed as describing sputtering appears in Tsushima.

The Office action cited [0031] of Tsushima as depositing the primer layer by sputtering. For convenience [0031] of Tsushima is repeated here:

> [0031] Next, a liquid containing a salt of a metal having a low standard electrode potential, e.g., a liquid containing a palladium salt, is brought into contact with the photosensitive layer 2 for adsorption of palladium in the exposed portion 2c of the channel portion 2b, as shown in FIG. 2(f). The palladium salt, when contacted with the exposed portion 2c where silanol groups have been produced, is chemically reduced to metallic particles of palladium which are subsequently adsorbed in the exposed portion 2c. On the other hand, such metallic particles of palladium are not produced in areas outside the exposed portion 2c, where the palladium salt can be readily removed by washing. Therefore, palladium is allowed to adsorb only in the exposed portion 2c. Also in the case where the metal colloid is used, it is possible to allow the metal colloid to selectively adsorb only in the exposed portion 2c.

The foregoing paragraph teaches a process in which silanol groups (e.g., Si-OH) are formed by a chemical reaction and then the silanol is reacted with a

palladium salt, as a result of which the palladium becomes bonded to the substrate. This is not sputtering. Sputtering is defined as follows:

> *Sputter deposition is a physical vapor deposition (PVD) method of depositing thin films by sputtering, that is ejecting, material from a "target," that is source, which then deposits onto a "substrate," such as a silicon wafer.* (Wkipedia: "sputter deposition")

Accordingly, Applicants respectfully submit that, in addition to the reasons the rejections of the claims should be withdrawn as discussed above with respect to all of the pending claims, the rejection of claim 12 as set forth in the Office action is clearly erroneous and without the support of any evidence, and therefore must be withdrawn.

New Claims 23 and 24

New claims 23 and 24 have been added. New claim 23 recites that the trenches and vias have a V-shape cross-section. This facilitates the electrolytic deposition of metal in the trenches and vias since the depth of the notches is small with respect to the width of their openings. New claim 24 recites that in method step c) the laser ablation comprises contacting the dielectric layer with a reactive gas during the laser ablation. This significantly enhances the speed with which the laser ablation can be carried out.

Applicants respectfully submit that claims 23 and 24 should be allowable for the same reason as all of the other pending claims, and because these claims recite additional features and benefits of the present invention.

Supplemental IDS

Applicants submit herewith a supplemental IDS, to cite an official action (dated 2010 February 5) of the Japanese Patent Office and references cited therein in a corresponding Japanese national phase application. English abstracts and partial translations are included. Appropriate consideration and indication thereof is respectfully requested.

CONCLUSION

Claims 1-24 are believed to be in condition for allowance. Notice to such effect is respectfully requested.

In the event any issues remain in the application, or if the Examiner considers that a telephone interview would facilitate the examination process, Applicant's undersigned attorney invites the Examiner to telephone him at the Examiner's convenience.

The fee for two additional total claims is submitted herewith. In the event any other additional fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 18-0988 under Attorney Docket No. **EFFEP0101US**.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

/thomaswadams/
Thomas W. Adams
Reg. No. 35,047

1621 Euclid Avenue, 19th Floor
Cleveland, Ohio 44115
Tel: 216-621-1113
Fax: 216-621-6165